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Silicon Structures for Power Electronics

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Abstract

In the present communication we consider the major requirements to the properties of low-doped working layers of multiplayer structures used in manufacturing power high-voltage transistors, thyristors and IGBT devices, which are the most widespread types of high-power high-voltage discrete devices. It is demonstrated experimentally how the non-uniformity of thickness and resistivity of the low-doped working layer can affect the parameters of high-power MDS transistors. We analyse the reasonability of using two- and three-layered structures formed by direct bonding, involving neutron-doped silicon grown by floating zone melting (FZ-Si) for the working low-doped layer, in manufacturing power electronic devices with U_{break} > 800 V. It is demonstrated that an alternative for FZ-Si can be silicon, grown according to Czochralski technique under an applied magnetic field (CZM), with oxygen content < $(4–5)10^{17}$ cm^{-3}.

INTRODUCTION

At present, the basic material for the production of practically all the major types of high-power high-voltage semiconductor devices is silicon; this situation will be conserved for at least the first decade of the 21st century.

Active part of high-power high-voltage devices (U_{br} > 100 V) is formed mainly from silicon with the resistivity of 20 W cm and higher; the higher is the working breakdown voltage of the device, the more should be resistivity of silicon. For modern discrete high-voltage devices, it is typical that, on the one hand, the size of chip increases as a result of passing from a multicrystal version to single crystal one; on the other hand, the minimal topological dimensions of the devices decrease; the major part of high-power discrete devices and high-power integrated circuits (IC) is formed planar on silicon substrate. As regards traditional thyristors, their foundation may be the whole silicon wafer.

Major characteristics of high-power high-voltage semiconductor devices are working voltage, current and commuted power; for field-effect and bipolar transistors, and thus IC based on them, major characteristics also include permissible parasitic currents: for bipolar transistors – leakage current I_{leak}, for field-effect transistors – residual current I_{res} determining the ideality of the reverse branch of VCC of the devices. For bipolar transistors operating with minority carrier charge, the reason of low percentage of proper chips, especially for high-power transistors for HF and SHF regions with low thickness of base, is often the increase of leakage current above the permissible level, connected with the presence of the defects in the base of the device; these defects lead to the localization of heat fields and to the secondary breakdown. The reason of low yield of bipolar transistors because of emitter-collector leakage may be both the transformed growth defects of the material (for example, defects of epitaxial film) and defects formed during the manufacture of the device, for example dislocations of the emitter edge. Besides, in high-power bipolar transistors operating in the key mode, in order to achieve quick operation of the device, it is necessary to provide short lifetime of minority carrier in the base region, which is achieved, for example, by introducing radiation defects by irradiaton of the device. So, to provide the required parameters, reliability, and efficien-

cy of production for this type of devices, the possibility is necessary to govern structural features of the active regions of bipolar transistors. As regards the defects leading to the worsening of the reverse branch of VCC ("soft" characteristics), for instance, we obtained direct correlation between the densities of small precipitates (30–40 nm) in the initial epitaxial films (presumably precipitates of iron or quartz) and the yield chips of multi-emitter power bipolar transistor of the HF range at the stage of the control of static amplification coefficient B_{st} and leakage currents $I_{c-â}$ (Fig. 1).

Since field-effect transistors operate with the majority carriers, large residual currents can be caused only by comparatively large structural defects at the boundary or in the vicinity of the *n–p* transition of the source region. In particular, we carried out the analysis that demonstrated the absence of any correlation between the densities of the observed types of structural defects in the working regions of the device (for high-power switching DM0S and VM0S transistors, the most widespread defect types are oxidation stacking faults (0SF) and coarse (9–12 mm) dislocation loops) and residual currents; only for $N_{def} > 10^4$ cm^{-2} the VCC of source diode was observed to worsen. High concentration of carbon and the presence of coarse precipitates of oxygen in the

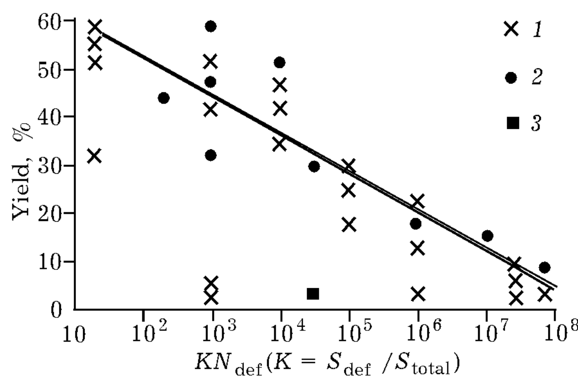

Fig. 1. The dependence of the yield of chips of bipolar transistors, formed on epitaxial structures, on the density of defects in initial epitaxial structures at the control stage B_{st} and I_{c-b} (acceptable: $B_{st} > 10$, $I_{c-b} < 10$ mA): *1* – the yield of chips on structures from one technological process of manufacturing the devices; *2* – on structures from different technological processes; *3* – the lot with high initial density of dislocations in the central part of structures ($N_{dis} > 1 \times 10^4$ cm^{-2}).

material can also lead to high residual current in this type of devices.

At the decrease of the degree of direct influence of structural defects on the parameters of devices for high-power field-effect transistors, IGBT devices, thyristors, very critical is the uniform distribution of doping impurity in the working layer, because one of the main characteristics, for example, of high-power MDS transistors, is the residual resistance of the conducting low-doped layer (R_{cond}), which determines directly the breakdown voltage of the transistor (U_{s-d}^{max}) and thus the scattered power. Besides, this resistance is also responsible for maximal switching frequency; in order to provide the working current of the device I_s^{max} (maximum source current), it is necessary not only to provide the correspondence of the resistivity of low-doped layer to the calculated value but also to provide minimal resistivity variation of this layer and the minimal thickness variation of this layer (Fig. 2). Besides, the main construction parameter of these transistors is known to be the total length of channel [1]; it is desirable to decrease it in order to decrease the size of the devices. When calculating the total length of the channel, it is necessary to take into account the real resistivity variation, and the thickness variation of the low-doped layer, both within one substrate and from one substrate to another in the lot. Because of this, the decrease of the variation of these two parameters of the working low-doped layers allows to carry out more precise calculations and to increase the yield transistors due to the decrease of the number of crystals with lower breakdown voltage. Calculations showed that the decrease of the resistivity and thickness variation of the low-doped layer from ± 20 to ± 5 % allows decreasing the length of channel of the device by a factor of 1.3, which is very important in solving the problem of decreasing the dimensions of high-voltage transistors.

The above considerations concerning the requirements to the uniformity of the resistivity of low-doped layer for MDS transistors is even more true for high-power thyristors. For example, in high-power thyristors with working voltage of several kilovolts the calculated resistivity nominal, for example 150 W cm,

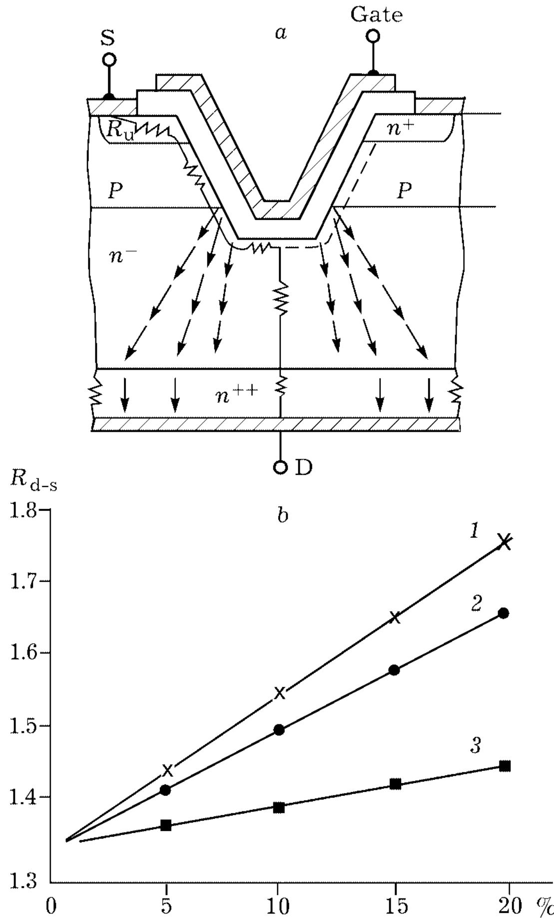

Fig. 2. The dependence of the drain-source resistance in the open state (R_{d-s}^{open}) on variation of thickness (Dh) and resistivity (Dr) of low-doped working layer of the n-channel high-power FETs: a – cross section of the transistor, b – dependencies for the cases: *1* – R_{d-s}^{open} = f(Dr and Dh), *2* – R_{d-s}^{open} = f(Dr) when Dh = 0; *3* – R_{d-s}^{open} = f(Dh) when Dr = 0.

should be retained at the silicon wafer 80 mm in diameter at an accuracy of several per cent.

For the major part of high-power devices, multilayer structures of the types n–n^+, p–p^+, n–n^+–p^+, *etc.* are used as initial substrates. The above considerations allow formulating rather clear requirements to the initial multilayered substrate structures for high-power MDS transistors, IGBT devices, thyristors:

– the resistivity variation (Dr) and thickness (Dh) of the low-doped active layer should not exceed ±5 % (however, desirable is a smaller per cent) of the calculated value;

– the density of defects with the size comparable to the depth of the n–p junction of the source in active regions of devices should not exceed $N_{def} < 1\times10^{4}$ cm^{-2}, especially in subsurface regions of the low-doped layer with a depth of $h = h_{js} + l_{OSF}$;

– the concentration of such impurities as oxygen and carbon in the low-doped working layer should not exceed $N_{[O_i]} < 6\times10^{17}$ xñm^{-3}, $N_{[C_s]} < 3\times10^{16}$ cm^{-3} [2];

– it is necessary to exclude the possibility of the formation of a parasitic n–p junction at the interface between the low-doped working layer and low-resistance layer during the formation of the device structures.

The major feature of the technological development of crystal production of high-power silicon devices at the present stage is that the traditional methods of manufacturing multilayer substrate structures: deep diffusion, direct and inverse epitaxy, are supplemented with a new technology based on direct bonding of silicon wafers, the so-called direct bonding process [3]. Naturally, world experience has already determined the efficiency of using these methods to manufacture multilayer structures for high-power devices: the new technology appears to be more efficient in manufacturing a series of high-power devices with breakdown voltage U_{br}> 800 V. In particular, as early as in 1991, some advanced companies declared that a step to "reasonable" high-power devices based on high-power MDS transistors is the transition to the new technology [4].

Surely, the choice of a definite technology of the formation of initial multilevel structures is determined by the economic efficiency of using one or another process of their preparation. Epitaxy or deep diffusion are traditional, well-mastered processes with available equipment to carry them out. However, the use of these processes in obtaining two- and three-layer initial structures with the upper low-doped layer of large thickness (80–130 mm) may be ineffective for some reasons:

– for deep diffusion, which is often used in the production of thyristors, because of high density of defects and because of the substantial variation of the thickness of low-doped layer as a result of "washing out" the diffusion front during doping at large depth, to say nothing of high consumption of electric energy;

– for epitaxy, because of auto-doping during the growth of thick low-doped films on strongly doped substrates [5]; the variation of

the thickness of low-doped layer when growing thick epitaxial layers; high density of defects in thick epitaxial layers; finally, the possibility for the appearance of the parasitic n–p junctions at the boundary between the layers when forming the devices, due to possible diffusion, for example, of the background boron admixture from the high-doped substrate into the low-doped part of the structure (in particular, our investigations showed that boron concentration in silicon doped of stibium with r = 0.01 W cm can exceed 1×10^{15} cm^{-3}).

The advantages of the technology of direct bonding of the wafers, in relation to power electronics, are as follows:

– low-doped working region is not the epitaxial layer but single crystal silicon with high structural perfection and, in case of correct choice of material, high structural thermal stability;

– the technology allows governing the concentration profile of charge carriers at the boundary between the layers of the structures to be formed by varying the regimes of processes of surface preparation for bonding (Fig. 3);

– the technology allows obtaining structures resistivity and thickness variation of the low-doped working layer by less than ±5 % at very clear coincidence of the resistivity of this layer with the calculated values.

Besides, the technology of direct bonding allows forming n–p junctions of large area which is of interest for the optimization of rectifier technology. In particular, using preliminary subdoping of the low-doped wafer, large-area diodes were manufactured, with the ideality coefficient 1.2–2.0 within the current density range 5×10^{-7}–5×10^{-1} A/cm^2, *i. e.* with the ideality coefficient of the known current dependence typical for usual diffusive n–p junctions with similar electric parameters [6].

The requirements to the initial multilayer silicon structures, verified during the studies, allow also determining the properties of silicon optimal for power high-voltage devices formed both in bipolar version and as field-effect transistors, and also for the modules and integrated circuits based on them:

– in the case when the epitaxial version is used for high-power devices as the material

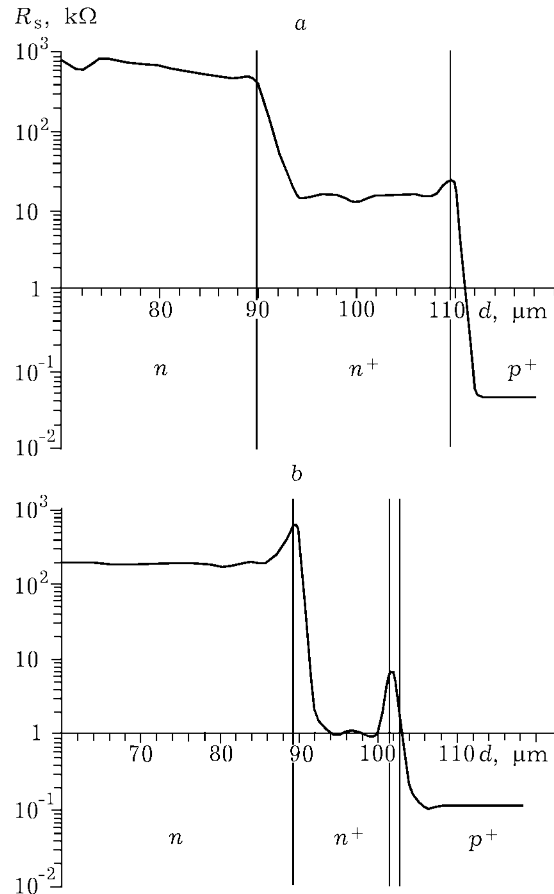

Fig. 3. Dependencies of the changes of spreading resistance (R_s) on depth at the boundary between layers in the $-n^+-p^+-$ structures obtained by the direct bonding process using silicon wafers: *a* and *b* – two different technological versions of forming multilayer structures.

for high-doped substrates should be silicon grown according to Czochralski technique with carbon content < 3×10^{16} cm^{-3} and with low content of residual impurities (their concentration should be less than the concentration of the doping impurity in the low-doped layer of the multilayer substrate);

– in the case when a single-layer substrate is used, or multilayer substrates formed by deep diffusion or direct bonding of the wafers for high-voltage transistors, IGBT devices, thyristors, high-voltage diodes, it is optimal to use low-doped neutron-doped silicon grown by means of floating zone method with carbon content not more than 1×10^{16} cm^{-3}. It is neutron transmutation doping that allows providing very high accuracy of obtaining the given resistivity (at an accuracy of 1 % and higher) and obtaining more uniform distribution of the impurity with minimal macro- and micro-

nonuniformity both in axial and in radial direction in the ingot, though neutron-doped silicon is surely more expensive than the material doped traditionally; at present it is practically impossible to carry out neutron doping of ingots with diameter more than 150 mm.

The technology of obtaining high-quality neutron-doped silicon is rather complicated, in particular, it is difficult to achieve high uniformity of neutron flux when the ingots several tens centimeters long and 100–150 mm in diameter are exposed, because the uniformity of the neutron flux should be higher than the required uniformity of the distribution of donors in silicon. The concentration of radiation defects formed during irradiation with neutrons is several orders of magnitude higher than the concentration of transmutation phosphorus; both the concentration and the properties of radiation defects, in particular their thermal stability, depend on irradiation conditions (dose of neutrons, temperature, ratio of fast to thermal neutrons), and on the properties of the initial silicon [7]. The use of silicon grown by the traditional Czochralski technique as an initial material for transmutation doping is not desirable because high oxygen concentration is present in this material, and the distribution of oxygen is nonuniform both along diameter and along the axis of the ingot. The defects caused by the presence of oxygen in the material can form under irradiation the charged structural distortions possessing high thermal stability. Besides, some "grown-in" microdefect of the crystal structure of the initial silicon, for example swirl defects, are able to capture phosphorus atoms, which prevents placing them in the lattice points and achieving the required uniformity of the specific resistance of the material.

There is one more danger connected with neutron doping, namely, the possibility of contamination during irradiation. Deactivation that is applied to remove surface radioactive contamination cannot always exclude the contamination of the volume, because some fraction of atoms adsorbed during irradiation from the water of the channel on the surface of samples can get into the subsurface region of the material during transmutation doping at sufficiently high fluences of thermal neutrons. In particular, sodium and gold, radioactive isotopes detected in noticeable amounts in the water of the channel, diffuse into the material even at small fluences of neutrons, especially sodium [8, 9].

An alternative to silicon grown by means of floating zone melting may be silicon grown in magnetic field with oxygen content less than $(4–5)\times10^{17}$ cm^{-3} (MCZ) [10]. Magnetic field increases the viscosity of silicon melt sharply (up to 6 orders of magnitude), which leads finally to the improvement of micro-homogeneity of the crystal. Besides, this method allows obtaining silicon ingots with oxygen content below 1×10^{17} cm^{-3} at more uniform distribution of this impurity over the ingot volume. This allows avoiding oxygen precipitation and formation of undesirable defects in the working regions of devices during thermal treatment of wafers.

We investigated eight slabs with diameter 76 and 100 mm grown in alternative magnetic field. In particular, with some ingots the following results were obtained: for the diameter 100 mm and the mass of 7 kg, oxygen content at the upper end was $[0_i]$ = (3.9 ± 0.9) %, at the lower end it was (2.8 ± 0.4) %; resistivity after neutron doping was (49 ± 5) % at the upper end and (48 ± 4) % at the lower end [9].

We carried out experimental investigation to find out what multilayer structures formed by direct bonding were optimal in manufacturing high-power high-voltage diodes with the area of $0.5´2$ mm^2 and DM0S *n*-channel transistors for 500 and 1000 V (working current 4–5 A); the material to form the working low-doped *n* layer in these structures was:

– silicon grown according to the Czochralski method at standard regimes;

– neutron-doped silicon grown by floating zone melting;

– silicon grown according to the Czochralski technique in variable magnetic field.

Besides, some devices were formed on multilayered structures obtained by direct bonding using low-doped silicon grown according to Czochralski in standard regimes, at the same time the silicon doped by stibium with r = 0.01 W cm with modifying admixture was used as a hith-doped material. In all the lots, the devices were manufactured

within a single technological process. Similar $n–n^+$ structures formed by epitaxial grown were used as the control structures.

Our investigations showed that only the use of multilayer structures obtained by direct bonding allowed us to obtain the devices of the class A when forming transistors with the breakdown voltage of 1000 V. The use of neutron-doped silicon as a material for low-doped layer in the formed substrate structures allowed us to increase yield the chips with the required breakdown voltage by a factor of 1.3–1.4 in comparison with similar substrates obtained epitaxially; the use of silicon with modifying admixture as a materials for the formation of the high-deped layer allowed us to avoid obtaining transistors with "soft" characteristics.

The efficiency of using one or another method to form the initial substrate structures for high-power high-voltage devices is illustrated in Fig. 4 showing the dependencies of the mean yield of the test high-voltage transistors with the voltage of 500 and 1000 V on the method of preparing the initial substrate structures; shown are also the cost of one such substrate and economic efficiency achieved in manufacturing chips for devices on the basis of substrate structures prepared by different methods. As one can see in Fig. 4, the use of the bonding substrate structures with neutron-doped silicon as a material for low-doped working layer allows one to save up to US $ 40–50 per every hundred chips of devices with U_{br} = 1000 V manufactured, in comparison with the results of using similar epitaxial structures.

The direct bonding process allows also forming the silicon on insulator (SOI) structures by bonding together the oxidated wafers in monolith so that a dielectric layer was between them. As a rule, this is a layer of thermal oxide. The development of the technology of obtaining these structures is also of interest for power electronics. In particular, the experts of Supertex Company (USA) proposed industrial method to form the "reasonable" high-power integrated circuit (Smart Power IC) intended for high current and voltage, on the basis of SOI structures obtained by direct bonding of silicon wafers (BSOI) [11]. When passing from

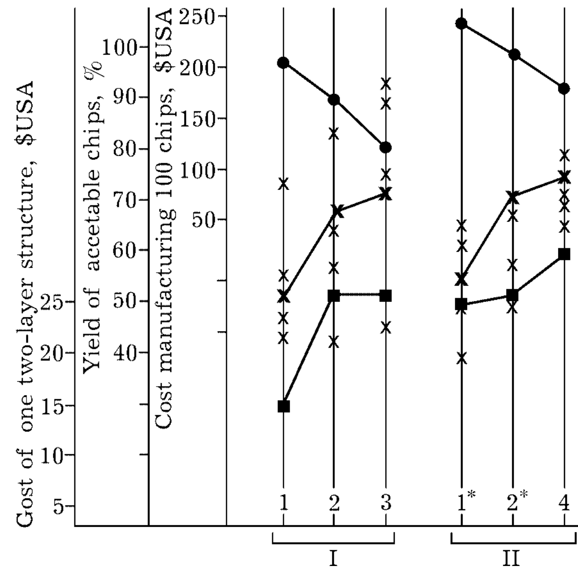

Fig. 4. Dependencies of the yield of chips (**X**), cost of one initial two-layer structure (■) and the cost of manufacturing 100 chips (·) of the test MOS transistors for 500 V (series I) and 1000 V (series II) on the method of obtaining initial two-layer structures: *1* and *1** – epitaxial structures; *2* and *2** – structures obtained by direct bonding using Si wafers that have been grown by the direct Czochralski method in standard regimes; *3* – structures obtained by direct bonding process using low-doped Si grown according to Czochralski method with applied magnetic fields; *4* – bonded structures involving low-doped neutron-doped floating zone Si.

the traditional structures with dielectric insulation (their cost being 150 dollars) to the structures manufactured according to new technologies, integrated circuits become of smaller size and the expenses for their manufacture decrease. These schemes contain single-operational thyristors and are a 40-channel driver for powerful displays, the output voltage of each channel being able to reach 300 V at the current of 300 mA. These circumstances play the decisive role in selecting high-power circuits manufactured using the direct bonding process, as the element base for the production of colour displays with flat screen, high-voltage operational amplifiers and equipment for communication means.

The results of mastering the industrial production of these circuits were presented at the international conference of electronic devices in 1997. The application of the direct bonding process allowed avoiding such traditional problems as undesirable "clicking"and slow switching of charging-discharging cycles in two-lay-

er structures manufactured using the direct bonding process.

CONCLUSIONS

1. The basic requirements to the features of the material for active regions of high-voltage bipolar and field-effect transistors are determined. It is demonstrated experimentally that large resistivity and thickness variation of the low-doped layer of multilayer initial structures can lead to the increase of the channel length and to the decrease of the yield of acceptable devices when forming high-voltage MDS transistors from these structures.

2. The basic technological versions of forming the initial multilayer structures used as substrates in manufacturing the major part of high-power high-voltage transistors, IGBT devices, thyristors are considered. It is demonstrated that it is efficient to use neutron-doped silicon grown by means of floating zone method or by the means Czochralski procedure under an applied magnetic field and at oxygen content less than $(4–5)\times10^{17}$ cm^{-3} for the formation of low-doped layers of multilayer substrate structures for high-power transistors with $U_{br} > 800$ V.

REFERENCES

1 V. V. Bachurin, V. P. Diakonov, A. B. Levin *et al., Elektrichestvo*, 3 (1986) 56.
2 M. Watanabe, *J. Solid State Technology*, March (1991) 69.
3 S. Bengtsson, *J. Electronic Materials*, 21, 8 (1992) 841.
4 Albleiter im Jahre 2000, *Elektronik Industrie*, 11 (1992) 102.
5 R. V. Kharlamov, Yu. A. Mikhailov, *Materialy elektronnoy tekhniki*, 1 (1999) 22.
6 V. M. Volle, V. B. Voronkov, I. V. Grekhov, V. A. Kozlov, *Pis'ma v ZhTF*, 15, 18 (1989) 59.
7 Neitronnoye transmutatsionnoye legirovaniye poluprovodnikov, in J. Mees (Ed.), Mir, Moscow, 1982, p. 262.
8 T. P. Svistel'nikova, V. A. Kharchenko, A. A. Stuk, *Neorgan. materialy*, 23, 1 (1987) 152.
9 T. V. Moiseenkova, T. P. Svistel'nikova, A. A. Stuk, *Ibid.*, 26, 1 (1990) 5.
10 V. B. Osvensky, V sb.: Fundamental'nye problemy rossiyskoy metallurgii na poroge XXI veka, izd. RAEN, Moscow, 1998, vol. 4, p. 85.
11 K. L. Enisherlova, Yu. A. Kontsevoy, *Materialy elektronnoy tekhniki*, 4 (2000) 4.