

A Project of Bipolar Field-Effect Transistor (IGBT) 50 A 1800 V Manufactured on the Plates of High-Resistance Crucible-Free Silicon with the Orientation (100)

EUGENIE V. CHERNYAVSKY¹, VLADIMIR P. POPOV¹, YURI S. PAKHMUTOV², YURI N. MIRGORODSKY³
and LEONID N. SAFRONOV¹

¹*Institute of Semiconductor Physics, Siberian Branch of the Russian Academy of Sciences, Pr. Akademika Lavrentyeva 13, Novosibirsk 630090 (Russia)*

²*Angstrom Co., Yuzhnaya promzona, Zelenograd, Moscow 103460 (Russia)*

³*Technological Center, MIET, Zelenograd, Moscow 103460 (Russia)*

E-mail: evgen@isp.nsc.ru

Abstract

A design of high-voltage IGBT transistor is proposed. The transistor is manufactured on a high-resistance substrate using the NPT technology. Numerical modeling of the manufacture and of the static voltage-current characteristics is carried out. The possibility to increase the working voltage to 1800 V is demonstrated.

INTRODUCTION

At present, power electronics is a rapidly developing area. Bipolar field-effect transistors with isolated gate (IGBT) are used as the major element in high-power switches [1–3]. The present work deals with the project of IGBT 50 A, 1800 V.

THE STRUCTURE OF THE DEVICE

At present, the plates of epitaxial silicon are used to manufacture high-voltage IGBT. However, the increase of the blocked voltage meets the necessity to increase the thickness of the epitaxial layer, which brings many technological difficulties. One of the methods to increase IGBT voltage is to use high-resistance silicon plates.

There are two approaches to the development of high-voltage IGBT. They involve the use of two structures: Punch Through (PT) [4, 5] and Non Punch Through (NPT) [6].

The structure of NPT provides more efficient time of IGBT switching off by creating

recombination centers in the collector region. The structure of PT provides the possibility to decrease the width of high-resistance N base by introducing N⁺ buffer in the collector region. One can see that both approaches have their own advantages. The structure NPT IGBT was selected for the project because it allows more efficient control of switching time, which leads to lower dynamic losses and better region of safe operation.

In order to manufacture IGBT 50 A 1800 V, the plates of crucible-free zone-melt silicon 4 inch in diameter are used; their orientation is (100), thickness 320 μm , specific resistance 120 $\Omega\text{ cm}$. Active area of IGBT according to the project is 0.4 cm^2 . Unit cell is square; its size is 20 \times 20 μm . The period of unit cell repetition is 40 μm . The view of unit cell is shown in Fig. 1. Total number of P⁺ emitters is 26 000. The width of the channel W of N channel MOS transistor is 3.1 μm .

To metallize emitter and contact to gate, aluminium 3 μm thick is used. Contacts are welded to emitter and gate with aluminium wire from the planar side. No special plates for welding current outputs to emitter are provid-

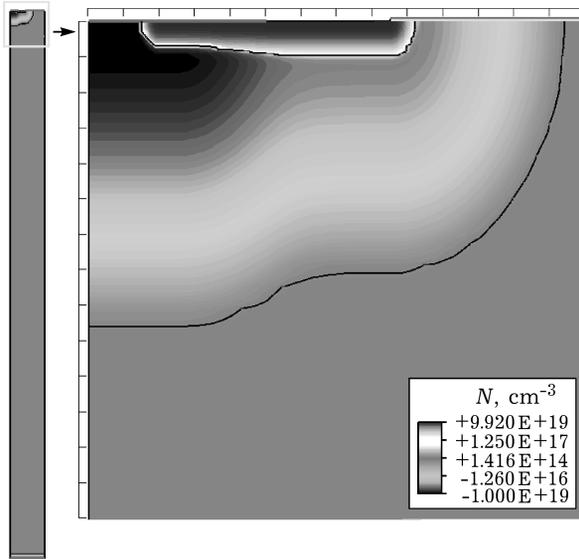


Fig. 1. The structure of the IGBT unit cell.

ed; the contacts are welded in any place over the emitter area. The collector is metallized with a three-layer structure Ti–Ni–Ag. Such a structure of the collector allows placing the crystal into the housing onto tin-lead solder.

In order to prevent breakdown over the crystal diameter the guard diffusion rings are used. Diffusion P rings manufactured according to the RESURF technology are used as guard rings [7]. The aluminium of the emitter is used as metal plates of capacitors while the passivating oxide of phosphorosilicate glass (PSG) is used as a dielectric. This technology was tested by us with a MOS controllable thyristors (MCT).

Using these parameters, a model was built up for IGBT fir which the current was calculated in the switched-on state and the leakages in the blocking state. This model corresponds to the device having a band topology and including half a band due to the symmetry. The results of modeling of the VCC are shown in Fig. 2. The calculated currents have the dimensions of $A/\mu m$; to determine total current, it is necessary to multiply the calculated value by the doubled total length of the strips.

The characteristics of the IGBT under design can be estimated using the results of numerical modeling. In Fig. 2, let us take $V_b = 16$ V. Saturation voltage corresponding to this voltage at the gate (base) is $V_{sat} = 4$ V. Hence, collector current will be $I_{coll} = 3.5 \cdot 10^{-5}$ A/ μm . Total current of the described IGBT will be

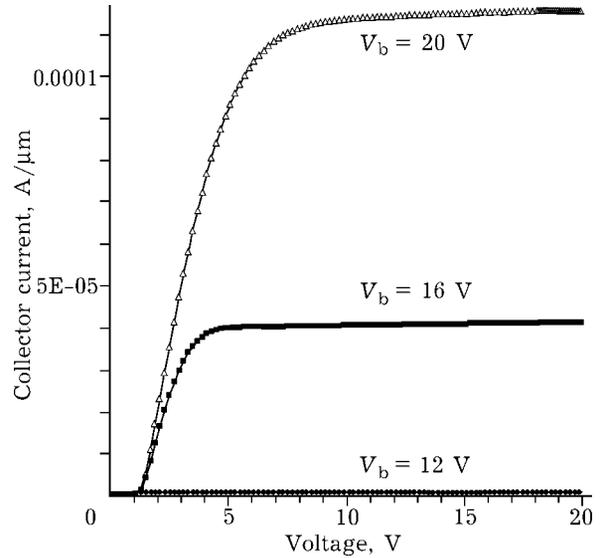


Fig. 2. The dependence of collector current on the voltage at the collector.

210 A. It should be noted that this model does not take into account the drop of voltage at contacts.

The blocked voltage at the gate voltage of $V_b = 0$ V was also calculated using this model. The results of the calculations are shown in Fig. 3. One can see that at the voltage of the collector above 1900 V the leakage current starts to increase exponentially. Leakage current of the device, calculated according to this plot, will be $I_{leak} = 18 \mu A$.

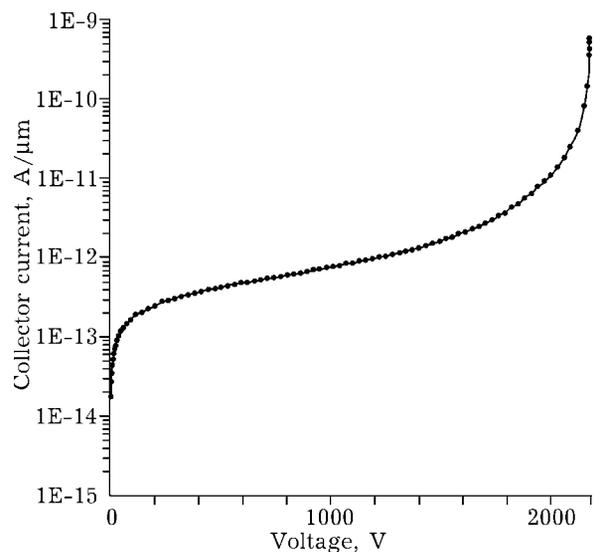


Fig. 3. The dependence of leakage current on the voltage at the collector ($V_b = 0$).

CONCLUSIONS

The above-described data demonstrate the possibility to create IGBT 50 A 1800 V on the basis of the plates made of high-resistance crucible-free silicon. According to the results of numerical modeling, a real possibility of creating such an IGBT is demonstrated. Static characteristics of IGBT are as follows: current, $I_{\max} = 200$ A; drop of voltage in the open state, $U_d = 4$ V, at $V_g = 16$ V. The selected structure of NPT IGBT has lower dynamic losses and larger region of safe operation. The use of crucible-free zone-melted silicon is a novelty, which allows one to reject epitaxial silicon plates. This makes the project much cheaper. In our opinion, this project deserves being embodied

as soon as possible at the Russian plants of microelectronics.

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