Latest Molecular Layer Epitaxy Technology

JUN-ICHI NISHIZAWA[1] and TORU KURABAYASHI[2]

[1]*Semiconductor Research Institute of Semiconductor Research Foundation, Kawauchi, Aoba-ku, Sendai 980-0862 (Japan)*

[2]*Telecommunications Advancement Organization, Sendai Research Centre, Koeji 19, Nagamachi-Aza Aoba-ku, Sendai 980-0868 (Japan)*

Abstract

As terahertz frequency devices, 100 Å scale ideal static induction transistor (ISIT) was fabricated with GaAs molecular layer epitaxy (MLE). The ISIT is estimated as electron transit time of $2 \cdot 10^{-14}$ s. In order to control the doping MLE at a sidewall in the fabrication process, the doping characteristics on each crystallographic orientation surfaces of GaAs substrate have been studied. In addition, the lateral growth rate on nanometre height step has been estimated by using table method. MLE of Si and SiO_2 layers were also tried with investigating the surface reaction by using *in situ* mass spectroscopy. For Si growth, temperature modulation (TM) method was performed using Si_2H_6 as source gas. SiO_2 thin layer was successfully deposited in Si MLE system by simultaneous supply of Si_2H_6 and active oxygen from helicon plasma source. Small temperature and pressure dependence of the deposition rate about 0.2–0.3 nm/min is useful for atomic and molecular level controlled process.

INTRODUCTION

Optical communication network systems with remarkable larger information capacity as terabit/s, 1000 times larger than conventional gigabit/s transmission are urgently required. In such demand, high speed devices operating in terahertz frequency should be developed. Static induction transistors (SIT) [1, 2] are suitable as terahertz devices. SIT is a kind of the field effect transistor with a very short channel, or the bipolar transistor with an ultimately thin base layer. In case the channel in SIT is made shorter than the mean free path of electrons, then injected electrons travel from source to the intrinsic gate without collision to lattice atoms [3]. This transistor was called "Ideal SIT". Later, Shur and Eastman estimated a similar cut-off frequency, and called the scattering-free transport as "ballistic" [4].

The GaAs ISITs with channels as short as 100 Å are achieved. An electron tunnelling through the potential barrier between the source and the drain of the transistor is a dominant transport mechanism.

The ISITs were fabricated with the molecular layer epitaxy [5], developed by J. Nishizawa who appreciated Suntola's idea of atomic layer epitaxy (ALE) for II–VI compound semiconductor polycrystals [6].

As a practical matter during the fabrication process of ISIT, a controlling of carrier concentration of doped layer and the thickness grown on the sidewall are significantly important for the difficulties of monitoring. As a basic research, crystallographic orientation dependence for MLE doping, and lateral growth on the sidewall have been studied. The doping characteristics show quite different manner in each oriented GaAs surface on (001), (111)*A* and (111)*B*. Such doping control is quite important for sidewall epitaxy in ISIT fabrication process. The growth of thickness on the sidewall was controlled by monitoring the growth on (001), however, a control of lateral growth has never been achieved. The size used in the quantum devices such as ISIT was several tens of nanometre order at the most. We have investigated the directional dependence of lateral growth on nanometre steps quantitatively by using table method [7].

Additionally, as new materials for application, MLE of Si [8, 9] with SiO_2 [10] deposition have been also developed to realize the

terahertz operating devices. At enough lower process temperature than conventional growth method, device quality epitaxial layers were achieved by molecular layer epitaxy.

IDEAL STATIC INDUCTION TRANSISTOR

The precision of MLE suits well for a fabrication process of 100 Å devices, as there is only 20 crystal cells between the source and the drain. In addition, the GaAs device quality crystal is grown at temperatures not exceeding 500 °C. The growth can be performed selectively on GaAs, without deposition on masked SiN layers. Epitaxial interface stoichiometry is well controlled, so that the selective epitaxial regrowth can be used as an advanced self-alignment method for fabrication of devices with channel lengths many times shorter than possible to achieve with definition by lithography. Vertical GaAs SITs with epitaxially regrown channel/gate structures were reported in other paper. For reducing the parasitic capacitance of transistors, double selective MLE regrowth was applied to fabricate an ISIT with source and drain arranged in a plane, on semi-insulating GaAs, so called horizontal ISIT as shown in Fig. 1. The thin $p^{++}(9 \cdot 10^{19}\ \mathrm{cm}^{-3})$ layer inserted between n^{++} $(5 \cdot 10^{19}\ \mathrm{cm}^{-3})$ source and drain layers induces a potential barrier. The two epitaxial interfaces meet in the channel of the device. The weak temperature dependence of the $I - V$ characteristics indicated the tunnelling electron current was dominant than the thermionic emission component [11–13]. The transconductance was 90 mS/mm. Minimization of the source/drain capacitance was verified by measurement of the $C - V$ dependence in such structure. Fitting the C to a model of double, sidewall and co-planar capacitance gave source-drain distances of 90–120 Å. The drift time of ballistic electron should not exceed $1 \cdot 10^{-14}$ s, then the sum of the tunnelling time and the drift time should be shorter than $2 \cdot 10^{-14}$ s. This value shows the operation of ISIT at terahertz frequencies.

MOLECULAR LAYER EPITAXY OF GaAs

The growth chamber was evacuated by a turbo-molecular pump, and the background pressure was about $1 \cdot 10^{-9}$ Torr. The arsenic source was pure AsH_3 (100 %), and the gallium source was pure TMG or $Ga(C_2H_5)_3$ (triethylgallium, TEG) without carrier gas. TMG (or TEG) and AsH_3 were introduced al-

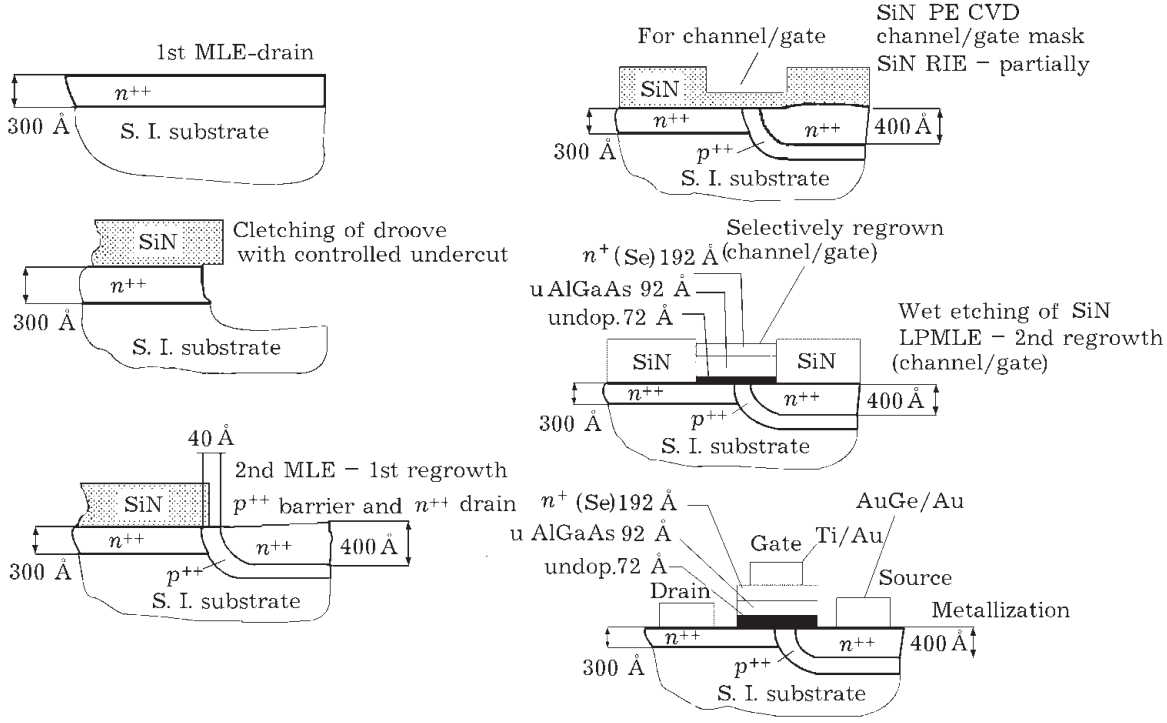
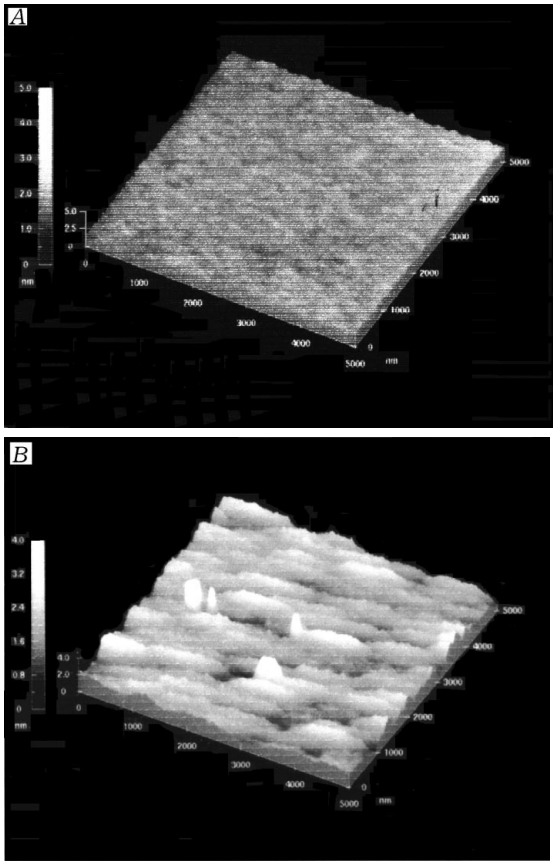


Fig. 1. Fabrication and structure of horizontal ISIT.



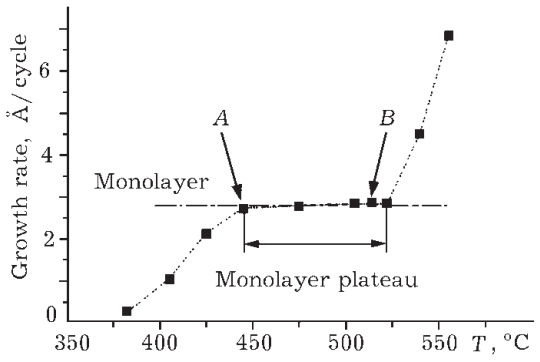


Fig. 2. Growth rate per cycle as a function of growth temperature and the surface roughness observed by AFM. *A*, *B* – growth temperature 445 and 514 °C, respectively.

ternately after being evacuated respectively. In the case of TMG – AsH_3 MLE, GaAs films are grown monolayer by monolayer [14].

Figure 2 shows the growth rate per cycle as a function of the growth temperature in TMG – AsH_3 MLE and the surface roughness observed by atomic force microscope (AFM). The growth sequence was 100"–4"–16"–4" a 100-s AsH_3 injection, a 4-s evacuation of AsH_3, a 16-s TMG injection, and a 4-s TMG evacuation. The injected TMG pressure was constant at $5 \cdot 10^{-5}$ Torr, and AsH_3 pressure was $1 \cdot 10^{-3}$ Torr. In the case of the temperature lower than 445 °C, the growth rate per cycle was less than the value of a monolayer, *i. e.* 0.28 nm/cycle. The self-limiting monolayer growth occurred at the temperature range from 445 to 534 °C (monolayer plateau). When the growth temperature was over 534 °C, the growth rate per cycle was over monolayer. The surface roughness as a function of the growth temperature was measured. When the growth temperature was over 470 °C in monolayer plateau region, the formation of the nucleated islands grown along the direction $[1\bar{1}0]$ was observed by AFM. However, when the growth temperature region was less than 470 °C in monolayer plateau, as shown in the figure at the growth temperature of 445 °C, the formation of such islands was not occurred and the smooth surface was observed in the order of monolayer accuracy.

DOPING TECHNOLOGY IN GaAs MOLECULAR LAYER EPITAXY

The effect of the doping period was studied experimentally in which the dopant source supplied during AsH_3 evacuation period (AA: after As), the TEG injection period (IG: in Ga), the TEG evacuation period (AG: after Ga), or AsH_3 injection period (IA: in As) [15]. The growth temperatures were 350–400 °C mainly. The electron concentration of the Se doped/n^{++} layer was controlled in the range of $4 \cdot 10^{18}$ to $3 \cdot 10^{19}$ cm^{-3} by changing the injection pressure and the duration of $Se(C_2H_5)_2$ (diethylselenium, DES) or $Te(C_2H_5)_2$ (diethyltellurium, DET) at the growth temperature of 400 °C.

In ISIT fabrication, at a sidewall of the chemical etched groove, the homojunction GaAs channel-gate (in vertical ISIT) and source-drain (in horizontal ISIT) structures were selectively regrown with MLE. The crystallographic orientation on the sidewall may be gallium stable surface like (111)*A*, or (311)*A*. For example, in the case of vertical ISIT fabrication, the five monomolecular layers thick n^{++} at the regrowth interface, induces a minimum in the potential barrier at the interface.

Normally-off and normally-on devices can be fabricated in the same process on GaAs, depending on crystal orientation of the channel-gate side-wall. In order to control the doping MLE at a sidewall, the doping characteristics on each crystallographic orientation surface of GaAs substrate have been studied. The AsH_3 supply in a cycle was 50 s at the partial pressure of $1 \cdot 10^{-3}$ Torr, and the TEG was 4 s at $7.2 \cdot 10^{-6}$ Torr. As a dopant gas, $Te(C_2H_5)_2$ was introduced for 2 s in a cycle at the partial pressure of $1 \cdot 10^{-7}$ Torr. Tellurium doped crystallographic orientation dependence on growth temperature has been studied. As the substrate, (100), (111)*A*, and (111)*B*-oriented undoped semiinsulating substrate were used. The doping characteristics show quite different manner in each oriented GaAs surface on (001), (111)*A* and (111)*B* as shown in Fig. 3. On Ga-stable (111)*A* surface, Te was doped at the lowest temperature in each orientation of the substrate. However, on arsenic-stable (111)*B* surface, Te doping was performed at the highest temperature. Doped Te should be incorporated in arsenic site, however, the arsenic stability on the growing surface should be different in each orientation of the substrate. For example, on (111)*A*, Ga is stable but not arsenic, therefore, Te might be incorporated at lower temperature, namely, doped Te is easy to desorb at higher growth temperature. Atomic concentration of Te measured by secondary ion mass spectroscopy (SIMS) shows the same tendency of temperature dependence as the carrier concentration on each orientation surface. The adsorption of Te or Te-compound on the growing surfaces is influenced strongly by the crystarographic orientations of the substrate.

These results indicate that the injection timing of DET in MLE growth is also important for site location of Te or Te-compound adsorbate on the surfaces. The injection period of DETe dependence on doping mode, AG, IA, AA and IG was examined as shown in Fig. 4. The doping mode dependence on (111)*A* shows the quite different manner with the one on (111)*B*. On (111)*A* surface, higher doping efficiency was achieved in the mode of IA (in As) and AA (after As). On this surface, arsenic is not stable, and the arsenic vacancy may be produced eas-

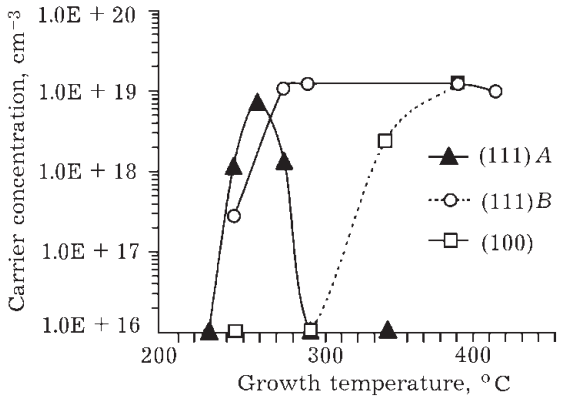


Fig. 3. Te doped crystallographic orientation dependence on the carrier concentration. *P*, Torr: $10^{-3}(AsH_3)$, $7.2 \cdot 10^{-6}$ (TEG), 10^{-7}(DET).

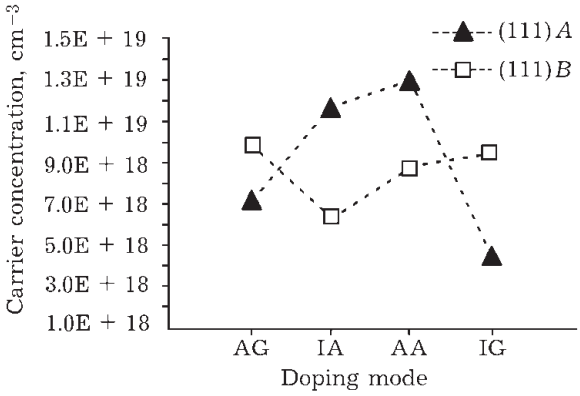


Fig. 4. Carrier concentration of Te doped (111) *A* (260 °C) and (111)*B* (383 °C) on each doping modes. *P*, Torr: $10^{-3}(AsH_3)$, $7.2 \cdot 10^{-6}$ (TEG), 10^{-7}(DET).

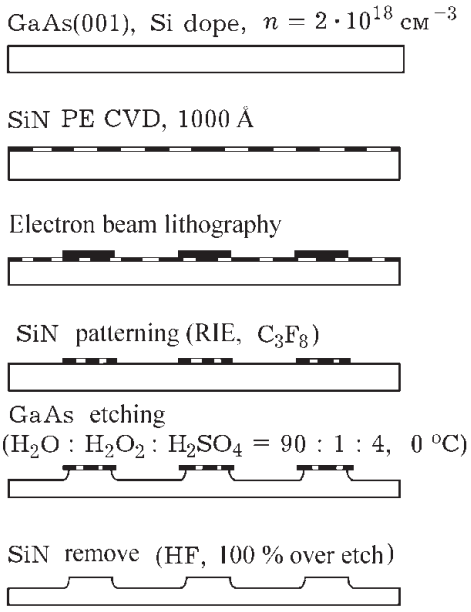


Fig. 5. Process chart for making the table pattern with 0.1 μm width and 15 nm height.

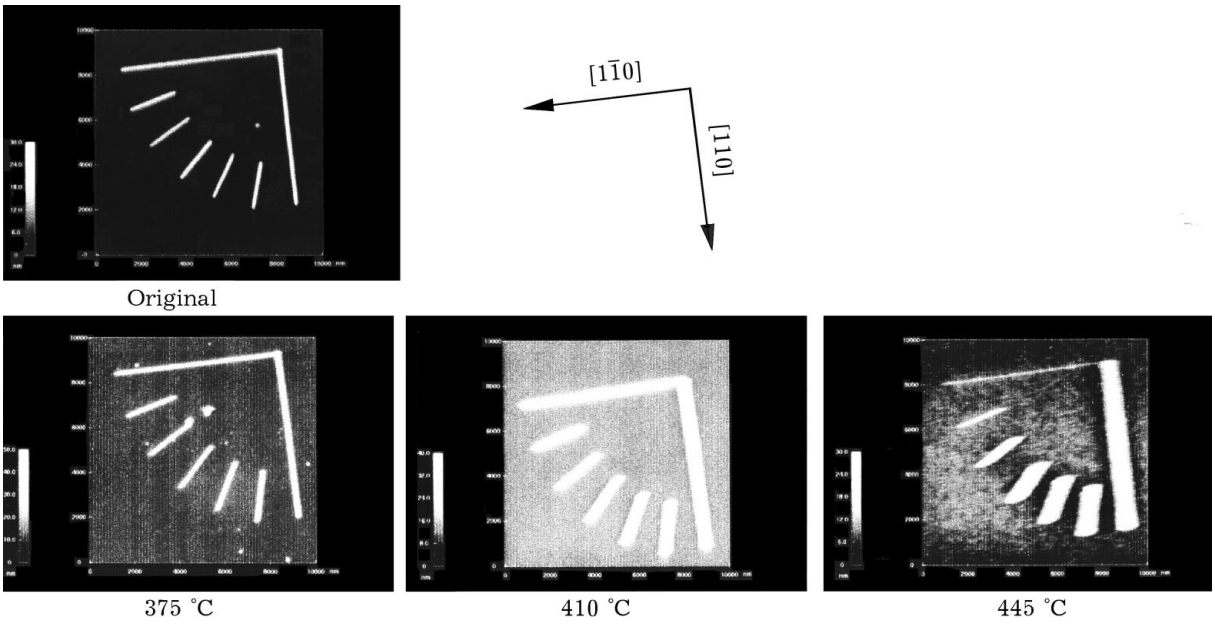


Fig. 6. Table pattern's AFM image before and after MLE.

ily at low temperature, then Te may be incorporated in the arsenic site. On (111)B, arsenic is stable, Te may be incorporated strongly on Ga atom directly as the doping efficiency is high in the mode of AG (after Ga) and IG (in Ga).

LATERAL GROWTH IN GaAs MOLECULAR LAYER EPITAXY

The directional lateral growth on the nanometre step of GaAs during molecular layer epitaxy was investigated quantitatively by using the table method [7]. In previous works on the table method, the table pattern size was a micrometre order, however, when we applied the table method to MLE, the miniaturization of the table pattern was required for a precise measurement of the lateral growth. So submicron size table pattern of GaAs was fabricated by using electron beam lithography. The pattern's line length and width were 5 and 0.1 μm, respectively. The height of the pattern was about 15 nm. The process chart for making the table pattern is shown in Fig. 5. It is as follows: (1) the substrate GaAs (001) doped with Si ($n = 2 \cdot 10^{18}$ cm^{-3}) was cleaned; (2) SiN plasma enhanced CVD for RJE mask was deposited; (3) electron beam lithography for making table pattern; (4) SiN C_3F_8 RIE; (5) formation of GaAs table pattern by wet etching; (6) SiN was removed. The table pattern's AFM image before and after MLE is shown in Fig. 6. The deformation was measured by using AFM and the lateral growth was estimated. The fastest lateral growth rate is in the [1$\bar{1}$0] direction and is 5–10 times greater than the vertical growth rate on GaAs (001) plane as shown in Fig. 7. The slowest lateral growth rate is in the [1$\bar{1}$0] direction and is nearly 0. With increasing the growth temperature, the lateral growth rate was increased in each direction. The deformation of the table pattern in each direction was proportional to sin θ (θ is the deviation angle from the [1$\bar{1}$0] direction on GaAs (001) plane). The deformation of lateral growth along the [1$\bar{1}$0] directions tends to increase followed by saturation with increasing the growth cycle. These results represent that the lateral growth

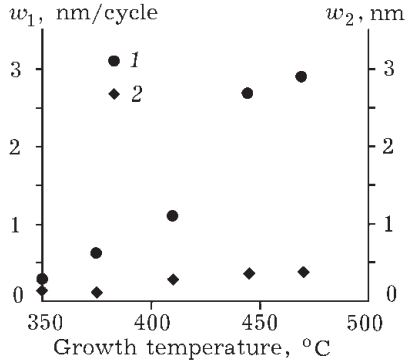


Fig. 7. The lateral growth (w_1) in the [1$\bar{1}$0] direction and the vertical growth rate (w_2) as a function of growth temperature: *1* – lateral growth rate, *2* – growth thickness.

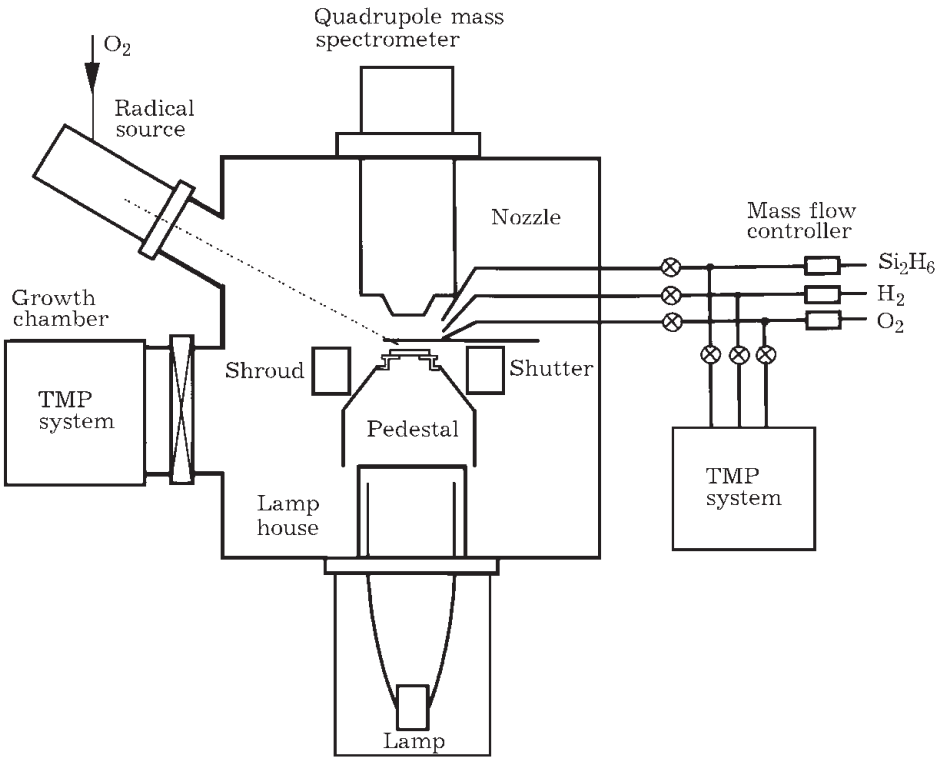


Fig. 8. Si and SiO_2 MLE system.

rate is proportional to the density of arsenic dangling bonds on the surface.

MOLECULAR LAYER EPITAXY OF Si and SiO_2

Si MLE has been performed by using $SiH_2Cl_2 - H_2$ system introducing SiH_2Cl_2 and H_2 alternately on the Si substrate at the temperature range of 800–900 °C [15]. However, the growth temperature over 800 °C is too high to fabricate nanometre scale devices such as ISIT. To reduce the growth temperature, Si_2H_6 was used as a source gas. The growth system is schematically shown in Fig. 8.

The MLE growth was performed by using temperature synchronized method, namely, the source gas injection was synchronized with the substrate temperature. In a cycle of gas injection, Si_2H_6 was introduced at the pressure of $1.3 \cdot 10^{-2}$ Pa for 10–100 s at the temperature of 400 °C, and the substrate was heated up to 550 °C and cooled to 400 °C within 30 s. Even when enough amount of Si_2H_6 was introduced at 400 °C, no growth occurred, therefore, the heating followed by the Si_2H_6 supply enables the surface reaction to proceed [9].

As shown in Fig. 9, mass spectroscopic measurement proves that the adsorption of Si–H compound is dominant at 400 °C after Si_2H_6 supply, and the hydrogen from the Si–H compound will be released by the surface reaction of $Si - H_x$ adsorbate when the substrate is heated up to 550 °C. By using the temperature modulation method, Si MLE was first accomplished at low temperature with self-limiting process as parameters of duration and/or pressure of Si_2H_6 supply as shown in Fig. 10. The thickness per cycle saturated at 0.4–0.5 Å/cycle which corresponded to about 0.3 monolayer, when Si_2H_6 supply was sufficient. The saturation tendency may correspond to the saturation of Si–H adsorption.

As related process with Si MLE, chemical vapour deposition of SiO_2 in high vacuum has also been studied by introducing Si_2H_6 and active oxygen (radical O_2) from helicon plasma source (13.56 MHz power of 200 W) in MLE system [15]. SiO_2 CVD was intended to fabricate MOS-gate structure in Si MLE chamber. At the partial pressure of $1 \cdot 10^{-2}$ Pa for Si_2H_6 and radical O_2, the deposition rate was nearly constant at 0.2 nm/min at the temperature range from 300 to 750 °C, while the oxidation speed

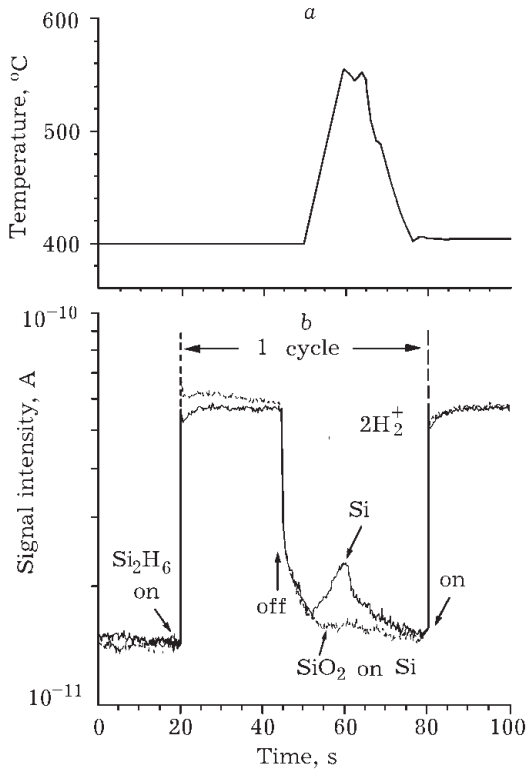


Fig. 9. Time dependence of controlled substrate temperature (*a*), and *in situ* mass spectroscopic signal of amu $2H_2^+$ (*b*).

was 0.04 nm/min with the same amount of radical O_2 introduced. Electrical characterization was done by metal – oxide – semiconductor structure with Al electrode for samples deposited at 500 °C. The maximum electric field at breakdown for SiO_2 was 10 MV/cm, and the interface state density was obtained at $3.5 \cdot 10^{11}$ cm^{-2}/eV from $C - V$ measurement. At the next stage, MOS gate structure by the CVD SiO_2 in Si MLE chamber, and the doping method in Si MLE will be applied to fabricate MOS gate ISIT structure.

CONCLUSION

MLE of GaAs has been developed to realize the terahertz operating devices with a basic research in the field of surface science and material science. As terahertz frequency devices, 100 Å scale ideal static induction transistor fabricated with GaAs molecular layer epitaxy is estimated as electron transit time of $2 \cdot 10^{-14}$ s. In GaAs MLE, the doping efficiency on each oriented surface, the lateral growth rate on nanometre height step, *etc*. have been estimated for precise control of device fabrication processes. In addition, MLE of Si and SiO_2 layers were also tried to actualize Si ISIT. For Si MLE, temperature modulation method was performed using Si_2H_6 as source gas. During growth the intensity of amu $2H_2^+$ were measured by *in situ* mass spectroscopy. It was clarified that the adsorption of Si–H compounds by Si_2H_6 supply and the desorption of hydrogen was successfully controlled by the TM method. The growth thickness per cycle of Si saturated at 0.4–0.5 Å/cycle which corresponded to about 0.3 monolayer on injection duration and on injection pressure of Si_2H_6, respectively. Furthermore, SiO_2 thin layer was successfully deposited in Si MLE system by simultaneous supply of Si_2H_6 and active oxygen from helicon plasma source.

The superior microwave performance will be presented soon in other paper. These studies are continued at Sendai Research Centre, TAO, Japan.

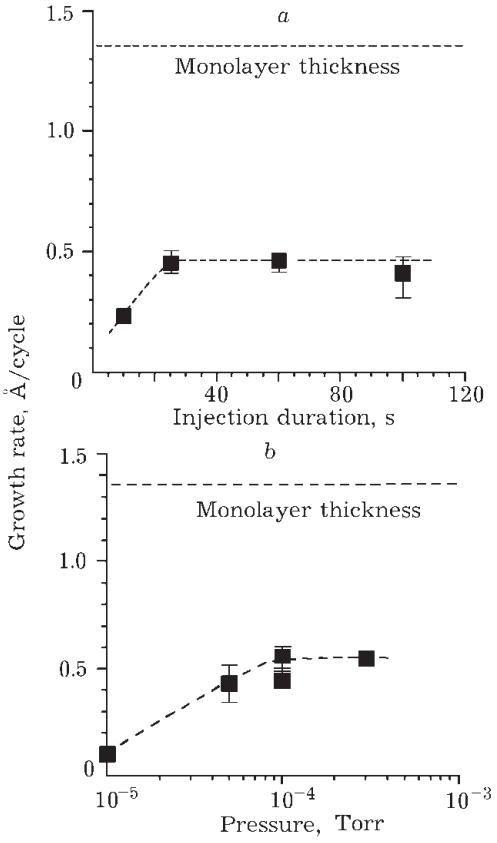


Fig. 10. Temperature modulation Si MLE. Si_2H_6 injection duration (*a*) and Si_2H_6 pressure (*b*) dependencies. Temperature modulation is 400–550 °C.

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